

SPECIFICATION AMENDMENTS

Page 7, lines 8-11, replace the paragraph with the following amended paragraph:

The invention does not use overvoltage identification devices with subsequent disconnection of the in-phase transistor, rather it is based on the principle of limiting the current in the in-phase transistor using its cut-off pinch-off voltage.

Page 9, line 20 through page 10, line 20, replace the paragraph with the following amended paragraph:

- a) in the event of a short circuit to ground potential GND ($V_{in} = 0V$), the voltage at the input E is also 0V and the protective circuit Ss operates normally.
- b) in the event of a short circuit to 14V (V_{bat1}) active at the device connection A, the source voltage V_s of the transistor T1 increases to a value $V_s = V_{bat1} - V_{th}$, in other words to a value $V_s < V_{bat1}$. The transistor T1 is now in the cut-off range pinch-off region. The current through the diode D3 is limited by the protective resistor R2 to a predefined permitted value.
- c) in the event of negative transient voltages (for example ISO test pulses) active at the device connection A, the transistor T1 becomes

conductive, with its gate source voltage V_{gs} now being limited by the Zener diode D1. The gate resistor R_V limits the current flow through the Zener diode D1 to a tolerable value. The protective resistor R2 limits the current flow through the diode D4 of the protective structure of the microcontroller μC .

- d) in the event of a short circuit to the 42V on-board electrical system active at the device connection A, the input voltage V_{in} increases drastically – up to maximum 60V. The source voltage V_s of the transistor T1 will increase in the event of a short circuit to 14V to a value $V_s = V_{bat1} - V_{th}$, i.e. a value $V_s < V_{bat1}$. As the transistor T1 is now in the cut-off range pinch-off region, the total voltage difference drops there to the input voltage V_{in} . The drain source voltage V_{ds} of the transistor T1 becomes $V_{ds} = V_{in} - (V_{bat} - V_{th})$. The power loss $P(T1)$ resulting at the transistor T1 is thereby determined by the voltage difference V_{ds} and the current $I(R2)$ flowing through the protective resistor R2: $P(T1) + V_{ds} \cdot I(R2)$. The peak value occurring with transient voltages of 60V is < 100mW, the effective value being around 60mW, which can be managed easily using a standard housing for the transistor T1.